

### **EU Project PICaboo to develop novel building blocks based on the generic foundry model that will transform the optical metro, DCI and access networks**

PICaboo “Photonic Integrated Circuits on InP technology pLAtform enaBling low cost metro netWOrks and next generation PONs”, a new EU-funded project under the H2020 ICT 2020- LEIT Photonics Call and the initiative of the Photonics Public Private Partnership, was launched at January 1st -2021, aiming to enhance PIC performances and reduce development costs by developing novel building blocks on the InP PIC platform of TUE and III-V Lab based on the generic foundry model. The project has duration of 3 years and a budget of 4,907,666.25 €. The project coordinator is the Institute of Communications and Computer Systems (GR) and it comprises a consortium of 6 partners; 2 top-of-rank universities Technische Universiteit Eindhoven (NL), and Institute of Communications and Computer Systems (GR), one world-class oriented research institute III-V Lab (FR), one world-leading design house VLC Photonics Sociedad Limitada (ESP) and two major industrial partners NOKIA Solutions and Networks GmbH & Co KG(DE) and ADVA Optical Networking SE (DE), from 5 European countries.

Indium-Phosphide (InP) Photonic Integrated Circuit (PIC) technology has been the workhorse for the development of optical transceivers for metro/core and access networks due to its high-speed operation potential and its capability for large scale monolithic integration. Despite its high-performance characteristics it is considered inherently an expensive technology compared to silicon photonics which relies on low cost CMOS processes. Significant efforts towards decreasing development costs and lowering the boundaries for fast prototyping is pursued via JePPIX pilot line, the EC manufacturing pilot line project for photonic integrated circuits based on InP, through open access to multi-project-wafer (MPW) runs from its foundries. Nevertheless, the performance of generic building blocks is often compromised since processes used for the development of a critical building block should not affect the performance of other building blocks cointegrated on the same PIC. The aggregation of multiple functionalities on a single chip is particularly important for bandwidth-hungry cloud and IoT applications considering that transceiver capacity can easily be increased via channel parallelization and multiplexing of the optical wavelengths, yielding in tandem significant cost benefits due to the reduced assembly complexity and its associated costs. This is where PICaboo steps in to develop novel building blocks based on the generic foundry model that will transform the optical metro and access networks in terms of speed, footprint, power consumption and cost. It will develop compact models of the building blocks and will compile them in process design kit (PDK)-compatible libraries allowing designers to explore their use in a wide range of applications hence maximizing their exploitation potential.

In more detail, PICaboo will develop a coherent optical receiver with reset-free phase and polarization control for low-cost metro and DCI applications within the range of 20-80 km. The

receiver PIC allows the migration of complex coherent digital signal processing (DSP) from the electronics to the optical domain and relies on the use of simplified DSP primarily employed in direct detection systems. In addition, PICaboo will develop an Electro-absorption Modulator (EAM) based Mach-Zehnder Modulator (MZM) and In-Phase and Quadrature Modulator (IQM) transmitter PICs with all-optical pre-equalization functionality on chip for 50/100 Gb/s and beyond PON applications. The embedded signal pre-equalization functionality will allow to increase PON speed complying with the optical distribution network power budget requirements and dispersion limit for 0-40 km. To develop its targeted PIC demonstrators, PICaboo will generate compact models for all its building blocks that will be included in libraries compatible to the platforms' PDKs after the end of the project. First validation of the building blocks via performance evaluation of PICaboo demonstrators will increase the technology readiness level (TRL) of the PIC platforms to >4 and will maximize the exploitation potential of the developed building blocks. PICaboo will exploit these models in order to explore the applicability of the building blocks in other applications too.

Driven by the latest industrial trends and technology standards, PICaboo aims to bring significant innovations in the fields of photonic integration technology, PIC design and photonics-enabled applications, targeting exploitation of its foregrounds after the project end into the relative markets and benefiting from emerging open market opportunities. It addresses the whole value chain targeting to turn its technological innovations into tangible products that will put Europe in the driver seat of optical transceivers' markets for metro/DCI and PON applications.

ICCS/NTUA apart from the role of the project coordinator, will bring in PICaboo its experience in system testing based on its state-of-the-art high-speed laboratory, system simulations and FPGA development and will be responsible for the development of the control electronics for PICaboo EAM-based transmitter PIC demonstrators and for the laboratory system-level performance evaluation of the developed EAM-MZM demonstrators.

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